UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/653,898	09/01/2000	Masahiko Kasashima	016907/1122	6519

22428 7590 06/18/2003

FOLEY AND LARDNER
SUITE 500
3000 K STREET NW
WASHINGTON, DC 20007

EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/653,898	KASASHIMA, MASAHIKO	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-20* is/are rejected.

7)☒ Claim(s) *6 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *0900* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Regarding the Abstract

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet **within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited**. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because **the Abstract is in excess of 150 words**. Correction is required. See MPEP § 608.01(b).

Rejections Based On Prior Art

3. The following references were relied upon for the rejections hereinbelow:

Nakase et al. (US 6,392,897 B1) Higashida et al. (US 6,328,572 B1)

The Indispensable PC Hardware Book (2nd edition, 1995; publishers: Addison Wesley) by Hans-Peter Messmer. [Hereinafter referred to as *The PC Hardware Book*)

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, 11, 12, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakase et al.

As to Claims 1, 11 and 16, Nakase et al. discloses, in Figs. 2, 3 and 4: a plurality of storage means 1a or 1b; means 10 for controlling storage means 1a or 1b (col.10: 23-28; means 12 and 13, having a resistance 12, for terminating an electric signal (col.10: 5-10); a pattern 11 in Figs. 2 and 3 (and comprising signal lines 11a and 11b in Fig. 4) electrically connecting storage means 1a or 1b, controlling means 10 and terminating means 12 and 13; wherein the plurality of storage means 1a or 1b, controlling means 10 and terminating means 12 and 13 are arranged on a board 9, and pattern wiring 11, 11a and 11b are located in a preset position on board 9 other than a position in which storage means 1a or 1b is located (Fig. 3 and col.10: 38-40; Fig. 4 and col.11: 36-37).

As to Claims 2, 12 and 17, Nakase et al. further discloses that wiring pattern 11 (Figs. 2 and 3), and wiring pattern 11a and 11b (Fig. 4), is located on an insulating portion of the board 9 surface, including the surface between the controlling means 10 and the terminating means 12 and 13 (Figs. 2, 3 and 4; col.10: 3-4; col.11: 36-37).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3, 4, 13, 14, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter referred to as *AAPA*) and Higashida et al.

As to Claims 3, 13 and 18:

I. Nakase et al. discloses that wiring pattern 11 (Figs. 2 and 3), wiring pattern 11a and 11b (Fig. 4), is arranged on a surface layer of board 9 and transmits the electric signal (col.10: 3-4; col.11: 36-37).

II. Nakase et al. does not teach that board 9 is composed of multiple layers.

III. *AAPA* and Higashida et al. disclose a board having memory modules mounted in connector sockets thereon, wherein the board is a multilayer board comprising 8 or more layers, including a ground layer and various bus line layers in order to provide the required circuit functionality for the system and impedance control for the signal bus lines interconnecting the memory modules (*AAPA*: p.2, lines 15-23; Higashida et al.: col.3: 63-co.4: 2).

IV. Since *AAPA* and Higashida et al. practice the same art of mounting memory modules on a motherboard as does Nakase et al., the use of a multilayer motherboard for carrying a higher density of functional circuitry and for controlling the impedance of

the bus lines using a ground layer would have been readily recognized in the pertinent art of Nakase et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the board of Nakase et al. to include multilayers of circuitry including bus lines and a ground layer, in order to increase circuit system functionality and control signal bus line impedance for the memory module assembly, as taught by *AAPA* and Higashida et al.

As to Claims 4, 14 and 19 modified Nakase et al. further discloses that the electric signal is transmitted from controlling means 10 to terminating means 12 and 13, and an impedance of the electric signal has a preset value (col.10: 57-60; col.12: 9-15).

8. Claims 5, 7-9, 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakase et al. in view of *AAPA* as applied to claims, 4, 14 and 19 above, and further in view of *The PC Hardware Book*.

As to Claims 5, 15 and 20:

I. Modified Nakase et al. does not explicitly teach a means for generating a clock signal.

II. *The PC Hardware Book* discloses that, in a memory system, physical memory access requires the coordination of, at the very least, the memory controller with other memory related functional circuitry (including buffer ICs) and the memory circuits (including memory ICs) in order to ensure correct read/write execution and that the individual circuits have enough time to fulfill their tasks, and that such coordination is carried out by clock signals (the paragraph bridging pp.141-142).

III. Since modified Nakase et al. has a memory controller 10 for accessing memory modules 1a or 1b (which include memory ICs 3 and buffer IC 6; see Fig. 1 and col.9: 63-65), then the problems of read/write execution and signal timing solved by a clock signal generating means, as taught in *The PC Hardware Book*, would have been readily recognized in the memory module system of Nakase et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a clock signal generating means in the memory module system of modified Nakase et al. and to supply the clock signal to the storage means connected to the terminating means in order to enhance the reliability of the memory module system of modified Nakase et al. by ensuring correct read/write execution and signal timing, as taught in *The PC Hardware Book*.

As to Claims 7 and 8, modified Nakase et al. further discloses, in Fig. 2, a plurality of storage means 1a including: a first storage means 1a (closest to controlling means 10) for receiving an output signal from controlling means 10, the first storage means 1a arranged to face an output terminal of controlling means 10; a second storage means 1a (to the right of the first storage means 1a), the second storage means 1a arranged to face an output terminal of the first storage means 1a, and an output terminal of the second storage means 1a arranged to face an input terminal of terminating means 12 and 13; wherein the pattern wiring 11 is at least arranged between the controlling means 10 and the first storage means 1a, between the first and second storage means 1a, and between the second storage means 1a and the terminating means 12 and 13 (Fig. 3 and 4 in conjunction with Fig. 2; col.10: 3-29). The

connectors 4a on the storage means 1a (or 1b) function as both inputs and outputs for data signals (col.9: 11-35) and connectors 4b on the storage means 1a and 1b function as both inputs and outputs for address/command signals (col.9: 36-50); the pattern wiring 11 is arranged between the terminals of the first and second storage means (Fig. 2; col.10: 1-13). With regard to the limitations of Claims 7 and 8, since the storage means (1a in Figs. 2 and 3; or 1b in Fig. 3) are identically wired and identically populated with the same memory and buffer chips (Fig. 1), and since the storage means are physically disposed in parallel with one another, the input terminals on the first storage means and output terminals on the second storage means, and the output terminals of the first storage means and the input terminals of the second storage means *inherently* are arranged to face each other.

As to Claim 9, since the storage means (1a in Figs. 2 and 3; or 1b in Fig. 3) are identically wired and identically populated with the same memory and buffer chips (Fig. 1), and since the storage means are physically disposed in parallel with one another (Fig. 2), then modified Nakase et al. further discloses, in Fig. 2, that only the output terminal of the first storage means (1a in Figs. 2 and 3; or 1b in Fig. 4) and an input terminal of the second storage means 1a (or 1b) among the terminals of the first and second storage means *inherently* are arranged to face each other, and the wiring pattern 11 is arranged between the first and second storage means (Fig. 2; col.10: 1-13).

Allowable Subject Matter

9. Claims 6 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim 6, patentability resides in *the second storage means being arranged on a reverse surface of the board*, in combination with the other limitations of the claim.

As to Claim 10, patentability resides in *the limitation wherein at least two of the plurality of storage means are individually provided in each of the front and reverse surfaces of the board*, in combination with the other limitations of the claim.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Mirov (US 6,008,682) discloses modules (including memory modules) 170 driven by a clock module 110 (Fig. 2; col.3: 59-col.4: 11).

b) Sanwo (US 5,530,623) discloses a motherboard 15 having memory modules 31-34 driven by controller 17 and a termination module 77 with termination resistor 75 and additional termination resistor 79 on motherboard 15 (col.4: 11-37).

c) Vogley et al. (US 6,028,781) discloses a memory bus 12 terminated by resistor 28 on a motherboard--not shown, but inherently present in order to electrically

and physically support the wires of memory bus 12 and the contacts of connectors 24--(col.4: 52-67).

d) Gasbarro (US 6,308,232 B1) discloses various on-chip, on-module and on-motherboard terminations 14 and 31 (Figs. 3 and 4; col.5: 21-41; col.6: 4-19).

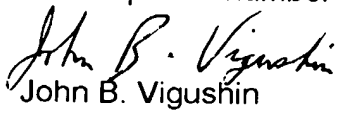
e) Wu (US 6,104,629) discloses a controller chip 24 and a memory module substrate 14 with memory modules 28 and a terminator chip 16, the controller chip 24 and module substrate 14 mounted on a motherboard 12 (Fig. 1).

f) La Rue (US 6,081,430) discloses a "loop-through" transmission line from motherboard 1 to memory module substrate 40 and back to motherboard 1, wherein the transmission line is terminated at both ends by termination resistors 9 (Figs. 4 and 7; col.3: 31-41).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



John B. Vigushin
Examiner
Art Unit 2827

jbv
June 10, 2003